CLAIMS

Having thus described our invention, and what we claim as new and desire to secure by Letters Patent is:

1. A method for characterizing circuit activity in an IC comprising: activating an IC, resolving the switching activity in space and time; generating a representation of the switching behavior which differentiates the time that circuits or transistors switch.

2. A method for characterizing circuit activity in integrated circuits (IC), comprising:

generating and applying signals to an integrated circuit (IC) to cause repeated switching activity in a region of interest in the IC, wherein said switching activity generates emissions from said region of interest;

recording data values identifying locations and times of said emissions;

assigning the emissions to circuit elements or devices in the region of interest;

processing the recorded data values to create emission waveforms; and

analyzing the emission waveforms to characterize circuit elements or devices in the region of interest.

3. A method according to Claim 2, wherein the signals are instruction sequences applied into memory elements of the IC under system operations, and the signals initiate execution of a sequence loop to cause repeated

stimulation of circuit elements or devices in the region of interest.

4. A method according to Claim 2, wherein the signals are a set of vectors or inputs applied to primary inputs of the IC.

5. A method according to Claim 2, wherein said switching activity generates optical emissions, and the recording step includes the step of recording time resolved optical emissions generated by the switching activity.

6. A method according to Claim 2, wherein the assigning step includes the step of using a layout vs. schematic (LVS) extraction to assign the emissions to the circuit elements or devices.

7. A method according to Claim 2, wherein the assigning step includes the step of automatically assigning the emission to the circuit element using information from a LVS extraction.

8. A method according to Claim 2, wherein the assigning step includes the step of semiautomatically assigning the emissions to circuit elements by having a user add or subtract circuit elements to the region of interest.

9. A method according to Claim 2, wherein the analyzing step includes the steps of:

analyzing the emission waveforms to identify timing and/or logic behavior; and

comparing said timing and/or logic behavior to behavior expected from electrical circuit stimulation.

10. A method according to Claim 2, wherein the analyzing step includes the steps of:

analyzing the emission waveforms to identify logic behavior; and

comparing said logic behavior to behavior expected from logic stimulation.

11. A method according to Claim 2, wherein the analyzing step includes the steps of:

using a known good circuit to obtain standard waveforms and/or image sequences; and

comparing the emission waveforms to said standard waveforms and/or image sequences.

12. A system for characterizing circuit activity in integrated circuits, comprising: means for activating an IC or system of Ics, means for detecting and recording the switching activity of the IC(s), and a means of representing the switching activities such that these may be characterized.

13. A system according to claim 12, further comprising an IC design viewer which provides a means to view the measured switching activity spatially and/or temporally.

14. A system according to Claim 13 further comprising means to identify and thereby relate the switching devices/circuits between the IC design viewer representations.

15. A system according to Claim 14 where the switching data is comprised of photon emissions and the IC design viewer is enabled to display emission images.

16. A system according to Claim 15, where the emission image(s) is(are) related to the design data (physical layout and/or circuit schematic and/or netlist).

17. A system according to Claim 15 where pixels, or other such units of areal designation are assigned to transistors or devices or circuits.

18. A system according to claim 17 where the pixels, or other such unit of areal designation, are assigned automatically by relating to the areal transistor/device/ckt designations.

19. A system according to Claim 17 where the pixels or other such units of areal designation are adjusted semi-automatically by a user interface whereby the user may indicate the pixels or regions desired for removal from, or addition to, the set of pixels or regions assigned to the device or transistor.

20. A system according to claim 19 where the graphical user interface enable "point and click" selection and deselection of pixels or regions.

21. A system according to Claim 19 where the graphical user interface shows questionable pixel or region designations where the user may wish to provide a choice.

22. A system according to Claim 15 where emission waveforms are viewable from the IC viewer.

23. A system according to claim 16 where emission waveforms are generated by a program from the areal designations per transistor, device, or circuit.

24. A system according to Claim 23 where the emissions waveforms are generated automatically when the user selects the option from the IC viewer control panel.

25. A system according to Claim 23 where the waveforms are generated automatically from the areal designations and are available for view either automatically or when requested, from the IC viewer.

26. A system according to Claim 21 where the waveform viewer and emission viewer are related and are cross probable.

27. A system according to Claim 22 where the waveforms and/or images are further viewable according to the design data hierarchy.

28. A system according to Claim 15 wherein clock distribution analysis and skew characterization is included.

29. A system according to claim 15 wherein areal regions are related to a common time-base by designation of a timing reference such as a reference signal contained in each region.

30. A system according to claim 29 which electronically combines regions to create a whole, or combined, visualization; the combined visualization may be in the form of a vide, still images, or waveforms.

31. A system for characterizing circuit activity in integrated circuits, comprising:

means for generating and applying signals to an integrated circuit (IC) to cause repeated switching activity in a region of interest in the IC, wherein said switching activity generates emissions from said region of interest;

means for recording data values identifying locations and times of said emissions;

means for processing the recorded data values to create emission waveforms; and

means for analyzing the emission waveforms to characterize circuit elements or devices in the region of interest.

32. A system according to Claim 31, further comprising a processor board for mounting the IC.

33. A system according to Claim 31, wherein the means for receiving the emissions includes an optical emission measurement system.

34. A system according to Claim 31, wherein the means for generating and applying the signals includes a system test computer.

35. A system according to Claim 31, wherein the analyzing means includes a computer.

36. A system according to Claim 31, wherein the means for generating and applying the signals includes an integrated circuit tester.

37. A system according to Claim 31, wherein the analyzing means includes an input for receiving a normal time-range input by a user.

38. A system according to claim 31, wherein the analyzing means includes a software utility for supplying normal time ranges.

39. A system according to Claim 31, wherein the analyzing means includes:

means for recording an expected behavior, including means for extracting from the waveforms a transition of a circuit element or device from a first state to a second state, and for recording an expected time for said transition from the application of a predetermined one of the signals.

40. A system according to Claim 31, wherein the region of interest includes input and output nets, each of the input and output nets having a logic state, and wherein the analyzing means includes means for recording a transition expected from the logic states at the input and output nets at a given time determined by a gate level simulation of the IC.

41. A system according to Claim 31, wherein the analyzing means includes means for flagging the occurrence of predefined peaks or the absence of predefined peaks, and said flagging means includes a software utility that compares the emission waveform to expected behavior data stored in a computer file.

42. A system according to Claim 31, wherein: the analyzing means includes means for flagging emissions that occur at wrong times; and said flagging means includes a software utility that compares the times of switching activity to expected times stored in a computer file, and that checks to determine if the switching activity is in a previously defined acceptable range.

43. A method for analyzing an integrated circuit, comprising:

detecting a fault in the circuit;

applying known stimulus to the circuit to reproduce the fault and to localize the fault to a component of the circuit:

collecting time resolved light emissions from the circuit component;

analyzing the collected time resolved light emissions to extract switching and timing data about the circuit components; and

comparing the extracted switching and timing data to expected switching and timing behavior data to characterize the fault.

44. A method according to Claim 43, wherein the comparing step includes the step of comparing extracted data to expected behavior data to identify (i) missing switching events, and (ii) switching events that should not have occurred.

45. A method according to Claim 43, wherein the comparing step includes the step of comparing extracted data to expected behavior data to detect early switching events and late switching events.